REMARKS

Examiner rejected claims 26-27, 29, 31, 35 and 39 under 35 USC 112, first paragraph, as lacking support in the specification.

Applicant traverses these rejections for the following reasons.

(a) With reference to claims 26 and 27, as well as to Fig. 3 of the original disclosure, the waveform of the "high-frequency output current" is depicted by Fig. 3D and identified as "CURRENT THROUGH L". As a person having but ordinary skill in the art pertinent hereto would readily perceive, this waveform has a "fundamental period"; which, in turn, has "a first and a second half-period". For instance, one of the half-periods could be identified as the positive portion of the waveform identified as "CURRENT THROUGH L".

Current flowing through "the first transistor" is the current depicted by Fig. 3C and labeled "TRANSISTOR CURRENT". As a person having but ordinary skill in the art can plainly see, this transistor current flows for "no longer than a brief span of time during each fundamental period". In fact, as actually depicted in Fig. 3C, this transistor current flows for a total duration shorter than one half (i.e., less than 50%) of the total duration of a complete half-cycle. Stated in another manner, during each complete fundamental period, this transistor current is prevented from flowing for a total duration that is longer than the sum of: (i) the duration of a complete second half-cycle, and (ii) half the duration of a first half-cycle.

Thus, without question (i.e., by a person having ordinary skill in the pertinent art), the original disclosure provides support for the recitation in claim 26 that "the second brief span of time [i.e., the time during which current is prevented from flowing through the transistor] is at least 10% longer than the duration of each half-period". (It is actually illustrated in Fig. 3C as being more than 50% longer than such duration.)

Likewise, with respect to claim 27, there is no question but that the original disclosure supports the recitation that "the first brief span of time is shorter than 90% of the duration of each half-period"; which "first brief span of time" is actually shown in Fig. 3D to be shorter than 50% of the duration of each half period.

Examiner rejected claims 25-40 under 35 USC 112, second paragraph as being indefinite.

Applicant traverses these rejections for the following reasons.

(b) In support for his rejections, Examiner refers claim 25 and the recitation therein that "each half-period being of substantially equal duration" and states that:

"The two halves just can't be of substantially equal duration for this would go against the meaning of the term half".

Applicant has no idea what Examiner refers to or what his problem is.

Clearly, with reference to the waveforms of Applicant's Fig. 3, particularly that of Fig. 3A, is it not immediately, totally and indisputably clear that "each half-period being of substantially equal duration".

Does perhaps Examiner believe that Applicant means that each half-period is equal in duration to that of the complete cycle? -- If so, Appliant informs Examiner to the effect that such a concern is inappropriate. Clearly, Applicant refers to the fact that the duration of each of the two half-periods is substantially equal to each other.

(c) Then, Examiner asserts that:

"Claim 25 is functional in nature".

It is unclear to Applicant what the significance of that phrase might be.

On basis of what authority does Examiner make this assertion?

In support of his position, Examiner further asserts that:

"The functional language beginning with with line 26 just does not have sufficient structure set forth in the claim so as to warrant the presence of the functional language in the claim".

Applicant disagrees with Examiner's assertion.

In fact, Applicant is unaware of any authority that might reasonably form the basis for Examiner's assertion.

Then, in further support for his position, Examiner states that:

"The claim does set forth a first transistor and that it conducts "current" in response to a control voltage that is provided at a control input. However, no means is set forth for

supplying that control voltage and thus no means is set forth that can enable the function of causing the first transistor to be "operative" to allow current to flow".

As would be clear to a person having but ordinary skill in the art, given the function recited in the claim, it is inherent that the structure defined by the claim include the particular means that Examiner holds to be missing.

That is, it would be unnecessary and redundant to state in the claim that the inverter means include a means functional to provide the control voltage.

Moreover, it is expressly permitted by 35 USC 112 to define an element in a multi-element claim as a "MEANS PLUS FUNCTION"; which implies that Applicant's "inverter means" is defined by way of the function ascribed to it; and, of course, providing the "first control voltage ... at a first control input" is part of that function.

(d) With respect to claim 24, Examiner states that:

"it does not positively recite the existance of means for the supplying of the recited first and second control voltages".

Applicant is unaware of any requirements to the effect that it is necessary to positively recite the existence of means for supplying the first and second control voltages. Clearly, as long as those control voltages are indeed being supplied, it is inherent that means must be present and so constituted and connected as to actually do so.

(e) The above arguments apply as well to Examiner's comments with respect to the indefiniteness of claim 28.

(f) With respect to claim 40, Examiner states that it:

"... is also indefinite for it does not positively recite that the control signal is indeed supplied to the transistor".

Again, Applicant responds by stating that he is unaware of any authority that requires the claim to be constructed in the particular manner apparently desired by Examiner.

Examiner rejected claims 25, 28, 30, 32-34, 36-38 and 40 under 35 USC 103 as being unpatentable over Dale et al. ("Dale") in view of Wotoweic and Stolz or Zansky.

Applicant traverses these rejections for the following reasons.

(g) With reference to the first paragraph at page 1 of the specification, the priority date for the subject matter of Applicant's claims is 08/14/80.

The priority date of Zansky is 11/26/80.

Hence, Zansky can not be used as a prior art reference against Applicant's claimed invention.

(h) With reference to the corrected lineage presented at page 1 of instant Amendment B, the priority date of Applicant's claimed invention is extended back to 12/28/78, at least with respect to the features against which Stolz is applied as a prior art reference.

The priority date of Stolz is 05/07/79.

Hence, Applicant's priority date of 12/28/78 is earlier than that of Stolz; which therefore obviates Stolz as a prior art reference against Applicant's invention.

CONCLUDING REMARKS

New claims 41-46 define various features which are neither disclosed nor suggested by any of the applicable cited references.

For instance, claim 43 defines a lamp assembly wherein the base includes a frequency-converting ballast means; which, in turn, includes an inverter operative to provide an inverter output voltage having an instantaneous magnitude that varies in accordance with the waveform illustrated by Fig. 3A.

None of the cited references describes or suggests an inverter having an output voltage of such particular nature.

Ole K. Nilssen, Pro Se Applicant